IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A Booth encoder circuit for generating Booth encoded output bits for a first multi bit binary input for use in a process including, in a selectable manner, either: multiplying together the first multi bit binary input and a second multi bit binary input, or multiplying together groups of bits of said first multi bit binary input and groups of bits of said second multi bit binary input where the first and second multi bit binary inputs are each partitioned into N groups, where N is an integer of two or more, the Booth encoder circuit comprising:

input connections for receiving a plurality of adjacent bits of the first multi bit binary input;

an encoder control input connection for receiving a control input for selecting between said multiplication of first and second multi bit binary inputs and said multiplication of said groups of bits of said first multi bit binary input and said groups of bits of said second multi bit binary input;

encoder logic to Booth encode said received bits of said first multi bit binary input to either generate unmodified Booth encoded output bits or modified Booth encoded output bits in dependence upon said received control input; and

output connections for outputting the generated Booth encoded output bits for use by selector logic to select a partial product bit in dependence upon the generated Booth encoded output bits and adjacent bits of said second multi bit binary input.

2. (Original) A Booth encoder circuit as claimed in claim 1, wherein the encoder logic comprises an arrangement of logic gates for encoding said bits of said first multi bit binary input, and said encoder control input connection is connected as an additional input for at least one of said logic gates.

3. (Previously Presented) A Booth encoder circuit as claimed in claim 1, wherein said encoder control input is arranged to receive a single bit control input.

4. (Previously Presented) A Booth encoder circuit as claimed in claim 1, wherein said encoder logic is arranged to set a plurality of bits of said modified Booth encoded output to a state dependent upon said control input.

5. (Original) A Booth encoder circuit as claimed in claim 4, wherein said encoder logic is arranged to set two bits of said modified Booth encoded output high in response to said control input.

6. (Previously Presented) A Booth encoder circuit as claimed in claim 1, wherein said encoder logic is adapted to generate said unmodified Booth encoded output bits as a plurality of bits indicating a multiplication factor to be used in calculating the partial product, and to generated said modified generated Booth encoded output bits as a plurality of bits at least one of which is set to a state dependent upon said control input.

7. (Original) A Booth encoder circuit as claimed in claim 6, wherein said encoder logic is adapted to generate one of said unmodified Booth encoded output bits to include a sign bit to indicate the sign of said multiplication factor and to modify said sign bit in dependence upon said control input in the generation of said modified Booth encoded output bits.

8. (Previously Presented) A Booth encoder circuit as claimed in claim 6, wherein said encoder logic is adapted to generate one of said unmodified Booth encoded output bits as a zero-indicator bit which takes the same value as the sign bit to select a multiplication factor of zero and which takes the opposite value to the sign bit to select a non-zero multiplication factor, and to modify said zero-indicator bit in dependence upon said control input in the generation of said modified Booth encoded output bits.

9. (Previously Presented) A Booth encoder circuit as claimed in claim 6, wherein said encoder logic is adapted to generate a subset of said unmodified and modified Booth encoded

output bits as one or more magnitude bits which indicate the magnitude of a non-zero multiplication factor.

10. (Previously Presented) A Booth encoder circuit as claimed in claim 1, wherein said input connections are arranged to receive three adjacent bits of the first multi bit binary input.

11. (Previously Presented) A Booth encoder circuit as claimed in claim 1, wherein said input connections are arranged to receive four adjacent bits of the first multi bit binary input.

12. (Previously Presented) A digital circuit for generating a partial product bit for use in a process including, in a selectable manner, either: multiplying together the first multi bit binary input and a second multi bit binary input, or multiplying together groups of bits of said first multi bit binary input and groups of bits of said second multi bit binary input where the first and second multi bit binary inputs are each partitioned into N groups, where N is an integer of two or more, the digital circuit comprising:

the Booth encoder circuit as claimed in claim 1; and

a selector having input connections for receiving adjacent bits of said second multi bit binary input and Booth input connections connected to said output connections of said Booth encoder circuit for receiving said generated Booth encoded output bits, and selector logic for selecting and outputting a partial product bit using said adjacent bits of said second multi bit binary input and said generated Booth encoded output bits.

13. (Original) A digital circuit as claimed in claim 12, wherein said selector logic comprises first selector logic having selection inputs connected to said input connections and at least one selector input connected to at least one of said Booth input connections for selecting from said adjacent bits of said second multi bit binary input on the basis of at least one said generated Booth encoded output bits, and second selector logic having selection inputs connected to a plurality of said Booth input connections and at least one selector input connected to the output of said first selector logic for selecting from said generated Booth encoded output bits on the basis of the output of said first selector logic.

14. (Original) A digital circuit as claimed in claim 13, wherein said first selector logic receives at least one generated Booth encoded output bit representing a multiplication factor to be used in the calculation of the partial product on said at least one selector input.

15. (Original) A digital circuit as claimed in claim 14, wherein said second selector logic receives two said generated Booth encoded output bits on said selection inputs, said generated Booth encoded output bits representing the sign of the multiplication factor and whether or not the partial product should be zero for unmodified generated Booth encoded output bits or two said generated Booth encoded output bits representing a state dependent upon said control input for modified generated Booth encoded output bits.

16. (Previously Presented) A digital circuit for processing a first multi bit binary input and a second multi bit binary input to generate partial product outputs in a process including, in a selectable manner, either: multiplying together the first multi bit binary input and the second multi bit binary input, or multiplying together groups of bits of said first multi bit binary input and groups of bits of said second multi bit binary input where the first and second multi bit binary inputs are each partitioned into N groups, where N is an integer of two or more, the circuit comprising:

a plurality of first digital circuits as claimed in claim 12; and

a plurality of second digital circuits, each second digital circuit comprising Booth encoder logic for receiving groups of bits of said first multi bit binary number and for generating Booth encoded output bits, and selector logic for receiving adjacent bits of said second multi bit binary input and said generated Booth encoded output bits and for selecting and outputting a partial product bit using said adjacent bits of said second multi bit binary input and said generated Booth encoded output bits;

wherein a first plurality of said first digital circuits are connected to a group of low significant bits of said first multi bit binary input, a group of high significant bits of said second multi bit binary input, and said control input, and a second plurality of said first digital circuits

are connected to a group of high significant bits of said first multi bit binary input, a group of low significant bits of said second multi bit binary input, and said control input;

a first plurality of said second digital circuits are connected to a group of high significant bits of said first multi bit binary input, a group of high significant bits of said second multi bit binary input, and said control input, and a second plurality of said second digital circuits are connected to a group of low significant bits of said first multi bit binary input, a group of low significant bits of said second multi bit binary input, and said control input.

17. (Original) A digital circuit as claimed in claim 16, wherein said groups of high and low bits comprise (M - M/N) bits, where M is the number of bits of said first and second multi bit inputs and N is the number of groups into which the inputs are selectably partitioned by said control input.

18. (Original) A digital device as claimed in claim 16 for performing computation including parallel partitioned multiplication, including control input generator logic to generate said control signal to select parallel partitioned multiplication.

19. (Original) A digital device as claimed in claim 18, wherein said control input generator logic is arranged to generate said control input as a plurality of bits indicative of the number of partitions for perform parallel partitioned multiplication using a choice of partition sizes.

20. (Previously Presented) A digital circuit for generating an output based on an operation involving multiplication of binary numbers comprising

a digital circuit as claimed in claim 16 for generating an array of partial products;
array reduction logic for reducing the number of partial products in the array; and
binary addition logic for adding the reduced partial products to generate an output.

21. (Original) A multiplication logic circuit comprising the digital circuit of claim 20 for multiplying at least one pair of binary numbers, wherein the output is the multiplication of said at least one pair of binary numbers.

22. (Original) A multiply-accumulate logic circuit comprising the digital circuit of claim 20, including logic for accumulating previous multiplications.

23. (Original) An integrated circuit comprising the digital circuit as claimed in claim 20.

24. – 45. (Canceled)

46. (Original) A digital circuit for generating partial product bits for use in parallel partitioned multiplication of a first input number by a second input number, the digital circuit comprising:

an encoder for receiving a plurality of adjacent bits of the first input number, a plurality of adjacent bits of the second input number, and a control input which indicates selection or non-selection of partitioned parallel multiplication, and for encoding said bits of the first input number to generate a control signal for use in selection of a partial product, said encoding including influencing the generation of said control signal when parallel partitioned multiplication is selected, such that the control signal is set to represent a partial product of zero; and

a selector for selecting a partial product bit using said bits of the second input number and said control signal;

47. (Original) A digital circuit as claimed in claim 46, wherein the encoder comprises an arrangement of logic gates for encoding said bits of the first input number to generate the control signal, and the control input comprises an additional input of at least one of said logic gates, such that the output of the logic gate is unaffected by the control input when partitioned parallel multiplication is not selected.

48. (Previously Presented) A digital circuit as claimed in claim 46, wherein said control signal comprises a plurality of control bits indicating the multiplication factor to be used in calculating the partial product.

49. (Original) A digital circuit as claimed in claim 48, wherein one of said control bits comprises a sign bit to indicate the sign of said multiplication factor.

50. (Original) A digital circuit as claimed in claim 48, wherein one of said control bits comprises a zero-indicator bit, which takes the same value as the sign bit to select a multiplication factor of zero, and which takes the opposite value to the sign bit to select a non-zero multiplication factor.

51. (Previously Presented) A digital circuit as claimed in claim 48, wherein a subset of said control bits are magnitude bits which indicate the magnitude of a non-zero multiplication factor.

52. (Previously Presented) A digital circuit as claimed in claim 46, wherein said plurality of adjacent bits of the first input number comprises three bits.

53. (Previously Presented) A digital circuit as claimed in claim 46, wherein said plurality of adjacent bits of the first input number comprises four bits

54. (Previously Presented) A digital circuit as claimed in claim 46, wherein said encoding comprises Booth encoding.

55. (Original) A method of using a digital circuit to generate partial product bits for use in parallel partitioned multiplication of a first input number by a second input number, the method comprising:

receiving a plurality of adjacent bits of the first input number, a plurality of adjacent bits of the second input number, and a control input which indicates selection or non-selection of partitioned parallel multiplication;

encoding said bits of the first input number to generate a control signal for use in selection of a partial product, said encoding including influencing the generation of said control signal when parallel partitioned multiplication is selected, such that the control signal is set to represent a partial product of zero; and

selecting a partial product bit using said bits of the second input number and said control signal.

56. (Original) A method as claimed in claim 55, wherein the encoding comprises:

using an arrangement of logic gates for encoding said bits of the first input number to generate the control signal, and

using the control input for an additional input of at least one of said logic gates, such that the output of the logic gate is unaffected by the control input when partitioned parallel multiplication is not selected.

57. (Previously Presented) A method as claimed in claim 55, wherein said control signal comprises a plurality of control bits indicating the multiplication factor to be used in calculating the partial product.

58. (Original) A method as claimed in claim 57, wherein one of said control bits comprises a sign bit to indicate the sign of said multiplication factor.

59. (Previously Presented) A method as claimed in claim 57, wherein one of said control bits comprises a zero-indicator bit, which takes the same value as the sign bit to select a multiplication factor of zero, and which takes the opposite value to the sign bit to select a non-zero multiplication factor.

60. (Previously Presented) A method as claimed in claim 57, wherein a subset of said control bits are magnitude bits which indicate the magnitude of a non-zero multiplication factor.

61. (Previously Presented) A method as claimed in claim 55, wherein said plurality of adjacent bits of the first input number comprises three bits.

62. (Previously Presented) A method as claimed in claim 55, wherein said plurality of adjacent bits of the first input number comprises four bits

63. (Previously Presented) A method as claimed in claim 55, wherein said encoding comprises Booth encoding.

64. (Original) A Booth encoder circuit for generating Booth encoded output bits for a first multi bit binary input for use in a process including, in a selectable manner, either: multiplying together the first multi bit binary input and a second multi bit binary input, or multiplying together groups of bits of said first multi bit binary input and groups of bits of said second multi bit binary input where the first and second multi bit binary inputs are each partitioned into N groups, where N is an integer of two or more, the Booth encoder circuit comprising:

input means for receiving a plurality of adjacent bits of the first multi bit binary input;

encoder control input means for receiving a control input for selecting between said multiplication of first and second multi bit binary inputs and said multiplication of said groups of bits of said first multi bit binary input and said groups of bits of said second multi bit binary input;

encoder means for Booth encoding said received bits of said first multi bit binary input to either generate unmodified Booth encoded output bits or modified Booth encoded output bits in dependence upon said received control input; and

output means for outputting the generated Booth encoded output bits for use by selector logic to select a partial product bit in dependence upon the generated Booth encoded output bits and adjacent bits of said second multi bit binary input.

65. – 66. (Canceled)